R6500

MICROCOMPUTER SYSTEM

R6500

Rockwell International

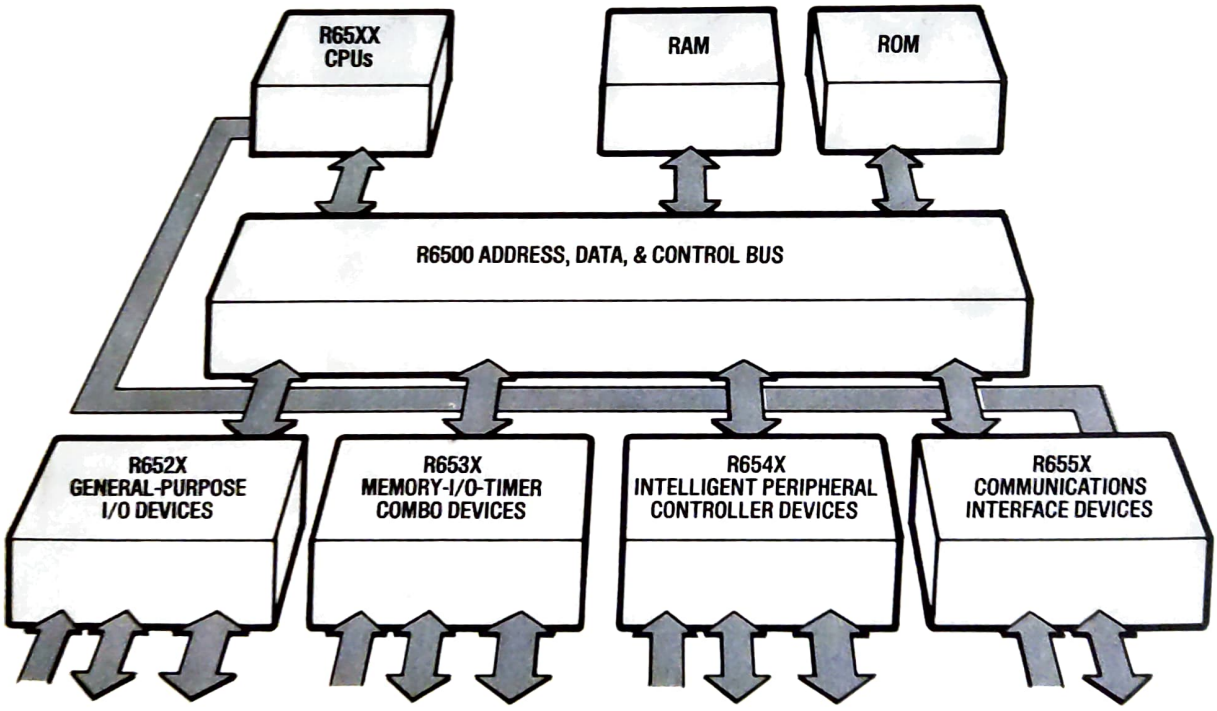
The R6500 Family

R6500 Family

A family of 10 software-compatible CPUs and 11 I/O, ROM, RAM and one-chip memory-I/O-timer circuits operating at proven 1 MHz and 2 MHz speeds with a single 5V power supply, provides you with economic system solutions for a broad range of applications.

The R6500/1 provides you with CPU, ROM, RAM, interrupts, counter and bi-directional data ports on a single chip. And it's totally software compatible with all other members of the R6500 family.

The R6500 promises you boosted performance and improved economics through its third generation architecture, which includes 13 powerful addressing modes, and its innovative circuit design and processing technology which reduce chip size and power consumption.



Rockwell is solidly backing the R6500

Rockwell has dedicated facilities for the high volume manufacturing of R6500 circuits produced with its own depletion load, silicon-gate N-channel process.

And Rockwell provides complete system development support: Rockwell's SYSTEM 65, a floppy-disk based, powerful yet low-cost complete development system. Plus AIM 65, TIM or timesharing program, complete documentation and extensive applications engineering support.

For the future, Rockwell is developing new R6500 devices that will enhance your own product development opportunities.

Rockwell's R650X CPU options offer a selection of features in 40- and 28-pin versions to meet your system needs (see table below). The R6502 - R6507 Series has on-chip clock generation. The R6512 - R6515 Series allows the user to generate and control the clock externally.

Why the R6500 is a cost performance winner

- Proven 1 MHz or 2 MHz performance
- Pipeline architecture for fast operation with fewer cycles
- Single 5-volt power supply
- On-the-chip clock or an external clock
- 56 instructions
- 13 addressing modes and true indexing capability
- Decimal/binary arithmetic mode selection
- Bi-directional Data Bus (compatible with the MC6800)
- Addressable memory range up to 65K bytes
- Multi-level interrupts – maskable/non-maskable
- Use with any type or speed memory
- Programmable stack pointer and variable length stack
- 40- and 28-pin DIP package options

R6500 CPU Options

	40-Pin DIP		28-Pin DIP				
	R6502	R6512	R6503 R6513	R6504 R6514	R6505 R6515	R6506	R6507
Memory Address Space	65K	65K	4K	8K	4K	4K	8K
Interrupts—Maskable —Non-Maskable	Yes Yes	Yes Yes	Yes Yes	Yes No	Yes No	Yes No	No No
SYNC—Output indicates op code fetch cycle	Yes	Yes	No	No	No	No	No
RDY—Single step and slow memory synchronization	Yes	Yes	No	No	Yes	No	Yes
$\emptyset_1$ Clock Output	Yes	Yes	No	No	No	Yes	No
DBE—Extended Data Bus Hold Time	No	Yes	No	No	No	No	No

The 40-pin versions provide full functional capability for memory intensive systems with extensive I/O requirements. The 28-pin versions offer flexibility in selecting the lowest cost CPU best suited to your application. 28-pin packages also provide denser board layout.

Thirteen addressing modes + true indexing = R6500 software power

The R6500 features 13 addressing modes. The first byte of each instruction is the operation code specifying both the instruction and the addressing mode. The addressing modes are summarized below.

- ACCUMULATOR ADDRESSING – A one byte instruction, operating on the accumulator.
- IMMEDIATE ADDRESSING – The operand is in the second byte of the instruction.
- ABSOLUTE ADDRESSING – The second and third bytes of the instruction specify the effective address in 65K bytes of addressable memory.
- ZERO PAGE ADDRESSING – Allows shorter code and execution times by assuming a zero page address.
- INDEXED ZERO PAGE ADDRESSING (X or Y, indexing.) – Zero page addressing used with an index register.
- INDEXED ABSOLUTE ADDRESSING (X or Y, indexing) – Absolute addressing used with X or Y index registers.
- IMPLIED ADDRESSING – The register containing the operand is implicitly stated in the operation code.
- RELATIVE ADDRESSING – Used only with branch instructions. The second byte is an "Offset" added to the contents of the program counter.
- INDEXED INDIRECT ADDRESSING – Uses an indirect zero page address indexed by X to fetch the effective address.
- INDIRECT INDEXED ADDRESSING – Uses a zero page address to fetch the effective base address to be indexed by Y.
- ABSOLUTE INDIRECT – Used only with JMP, the second and third bytes point to a two-byte effective address.

R6500 Microprocessor Instruction Set

		Execution Time (clock cycles)											
		Accumulator	Immediate	Zero Page	Zero Page, X	Zero Page, Y	Absolute	Absolute, X	Absolute, Y	Implied	Relative	(Indirect, X)	(Indirect), Y	Absolute Indirect
ADC	Add Memory to Accumulator with Carry	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
AND	"AND" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
ASL	Shift Left One Bit (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
BCC	Branch on Carry Clear	•	•	•	•	•	•	•	•	•	2**	•	•	•
BCS	Branch on Carry Set	•	•	•	•	•	•	•	•	•	2**	•	•	•
BEQ	Branch on Result Zero	•	•	•	•	•	•	•	•	•	2**	•	•	•
BIT	Test Bits in Memory with Accumulator	•	•	3	•	•	4	•	•	•	•	•	•	•
BMI	Branch on Result Minus	•	•	•	•	•	•	•	•	•	2**	•	•	•
BNE	Branch on Result not Zero	•	•	•	•	•	•	•	•	•	2**	•	•	•
BPL	Branch on Result Plus	•	•	•	•	•	•	•	•	•	2**	•	•	•
BRK	Force Break	•	•	•	•	•	•	•	•	•	•	•	•	•
BVC	Branch on Overflow Clear	•	•	•	•	•	•	•	•	•	2**	•	•	•
BVS	Branch on Overflow Set	•	•	•	•	•	•	•	•	•	2**	•	•	•
CLC	Clear Carry Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
CLD	Clear Decimal Mode	•	•	•	•	•	•	•	•	2	•	•	•	•
CLI	Clear Interrupt Disable Bit	•	•	•	•	•	•	•	•	2	•	•	•	•
CLV	Clear Overflow Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
CMP	Compare Memory and Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
CPX	Compare Memory and Index X	•	2	3	•	•	4	•	•	•	•	•	•	•
CPY	Compare Memory and Index Y	•	2	3	•	•	4	•	•	•	•	•	•	•
DEC	Decrement Memory by One	•	•	5	6	•	6	7	•	•	•	•	•	•
DEX	Decrement Index X by One	•	•	•	•	•	•	•	•	2	•	•	•	•
DEY	Decrement Index Y by One	•	•	•	•	•	•	•	•	2	•	•	•	•
EOR	"Exclusive OR" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5	•
INC	Increment Memory by One	•	•	5	6	•	6	7	•	•	•	•	•	•
INX	Increment Index X by One	•	•	•	•	•	•	•	•	2	•	•	•	•
INY	Increment Y by One	•	•	•	•	•	•	•	•	2	•	•	•	•
JMP	Jump to New Location	•	•	•	•	•	3	•	•	•	•	•	•	5
JSR	Jump to New Location saving Return Address	•	•	•	•	•	6	•	•	•	•	•	•	•
LDA	Load Accumulator with Memory	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
LDX	Load Index X with Memory	•	2	3	•	4	4	•	4*	•	•	•	•	•
LDY	Load Index Y with Memory	•	2	3	4	•	4	4*	•	•	•	•	•	•
LSR	Shift Right One Bit (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
NOP	No Operation	•	•	•	•	•	•	•	•	2	•	•	•	•
ORA	"OR" Memory with Accumulator	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
PHA	Push Accumulator on Stack	•	•	•	•	•	•	•	•	3	•	•	•	•
PHP	Push Processor Status on Stack	•	•	•	•	•	•	•	•	3	•	•	•	•
PLA	Pull Accumulator from Stack	•	•	•	•	•	•	•	•	4	•	•	•	•
PLP	Pull Processor Status from Stack	•	•	•	•	•	•	•	•	4	•	•	•	•
ROL	Rotate One Bit Left (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
ROR	Rotate One Bit Right (Memory or Accumulator)	2	•	5	6	•	6	7	•	•	•	•	•	•
RTI	Return from Interrupt	•	•	•	•	•	•	•	•	6	•	•	•	•
RTS	Return from Subroutine	•	•	•	•	•	•	•	•	6	•	•	•	•
SBC	Subtract Memory from Accumulator with Borrow	•	2	3	4	•	4	4*	4*	•	•	6	5*	•
SEC	Set Carry Flag	•	•	•	•	•	•	•	•	2	•	•	•	•
SED	Set Decimal Mode	•	•	•	•	•	•	•	•	2	•	•	•	•
SEI	Set Interrupt Disable Status	•	•	•	•	•	•	•	•	2	•	•	•	•
STA	Store Accumulator in Memory	•	•	3	4	•	4	5	5	•	•	6	6	•
STX	Store Index X in Memory	•	•	3	•	4	4	•	•	•	•	•	•	•
STY	Store Index Y in Memory	•	•	3	4	•	4	•	•	•	•	•	•	•
TAX	Transfer Accumulator to Index X	•	•	•	•	•	•	•	•	2	•	•	•	•
TAY	Transfer Accumulator to Index Y	•	•	•	•	•	•	•	•	2	•	•	•	•
TSX	Transfer Stack Pointer to Index X	•	•	•	•	•	•	•	•	2	•	•	•	•
TXA	Transfer Index X to Accumulator	•	•	•	•	•	•	•	•	2	•	•	•	•
TXS	Transfer Index X to Stack Pointer	•	•	•	•	•	•	•	•	2	•	•	•	•
TYA	Transfer Index Y to Accumulator	•	•	•	•	•	•	•	•	2	•	•	•	•

*Add one cycle if indexing across page boundary
**Add one cycle if branch is taken, and one additional cycle if branching operation crosses page boundary

R6500/1 One-Chip Microcomputer

The R6500/1

In the R6500/1, Rockwell has combined the high-performance R6502 CPU with such versatile features as 2048 bytes of ROM, 64 bytes of RAM, 32 bi-directional I/O lines, four interrupts and a 16-bit programmable counter (with four separate interval/event modes) — all in a single 40-pin package.

The R6500/1 also has on-the-chip 1 MHz or 2 MHz clock operation with external single clock, crystal or RC frequency input.

The R6500/1 includes a separate power pin that maintains RAM on 10% of the operating power. In the event power is lost, this standby power retains RAM data until execution is resumed.

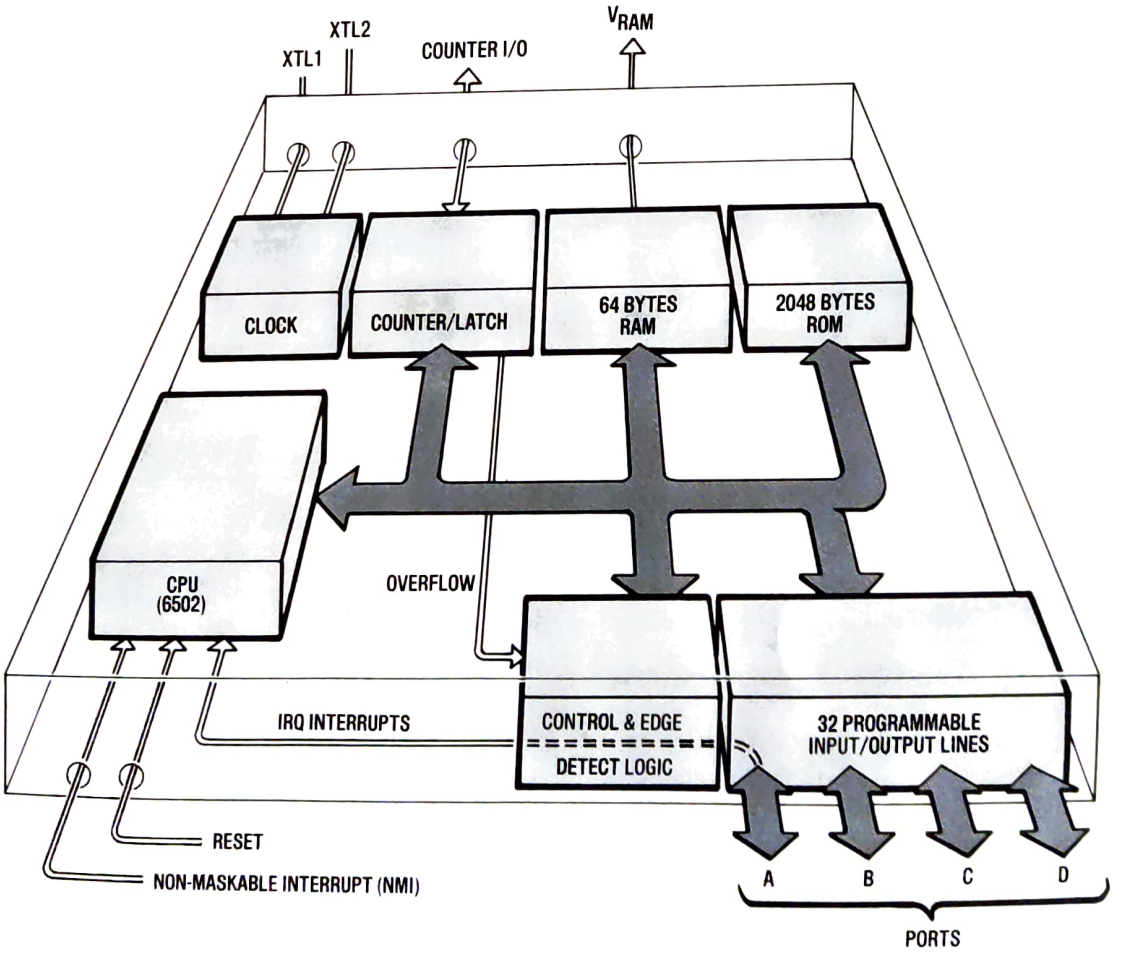
Rockwell backs up the R6500/1 with solid system development support in two ways:

The R6500/1E, a 64-pin emulator device with 40 pins electrically identical to the R6500/1, may be used for program development and prototyping with external EPROM or RAM.

A Personality option to SYSTEM 65 customizes Rockwell's popular microcomputer development system for complete R6500/1 software and hardware development.

R6500/1 Features

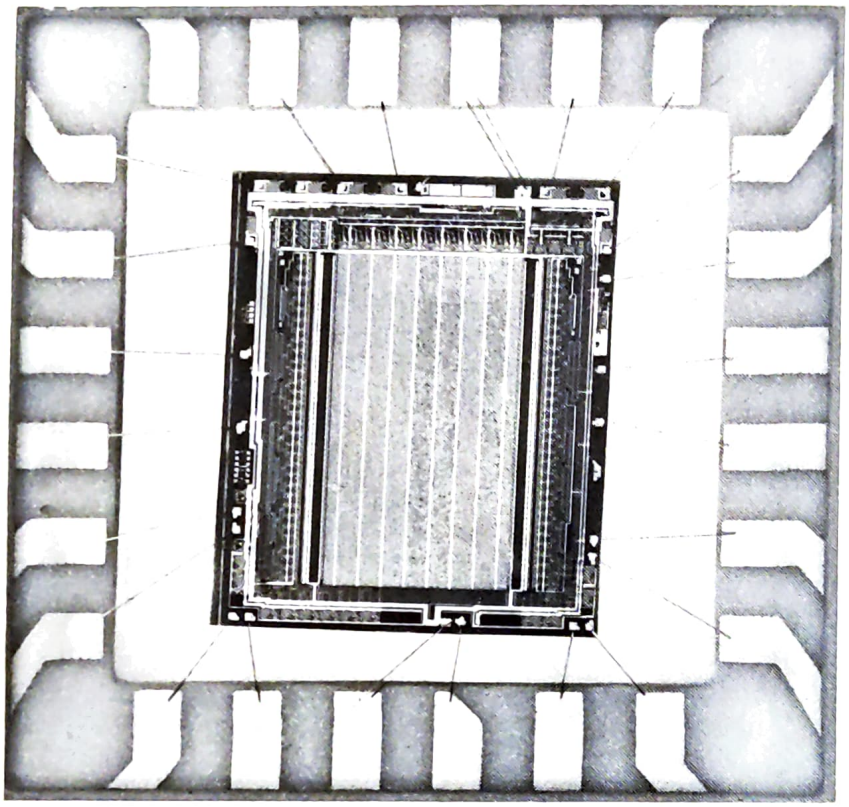
- 2K-Byte Mask Programmable ROM
- 64-Byte Static RAM
- R6502 CPU
- Four 8-Bit Bidirectional I/O Ports
- 16-Bit Programmable Counter/Latch With Four Modes:
  - — Interval Timer
  - — Pulse Generator
  - — Event Counter
  - — Pulse Width Measurement
- Five Interrupts
- Fully Upward/Downward Compatible With 6500 Family
- 64-Pin PROM-compatible Emulator Device Available



Standard Memory Devices

The R6500 system bus enables you to use low cost, widely available standard memory devices. For your convenience, Rockwell now offers the five memory devices, described below. All are completely TTL compatible, fully static — no clocks or refresh strobes required — and operate from a single + 5 V power supply

- **R2114 4K STATIC RAM**
  1024 x 4 in high-density 18-pin package with common data I/O; 450ns access and cycle time; fully static — no clocks or strobes required; single + 5V power supply; total TTL compatibility. (Industry standard.)
- **R2316B 16K STATIC ROM**
  2048 x 8 in standard 24-pin package; pin-compatible with 2708 EPROM; 450 ns. max. cycle time; three chip selects. (Industry standard; replaces *two* 8K EPROMs.)
- **R2332 32K STATIC ROM**
  The industry's first static 4096 x 8 N-channel ROM; standard 24-pin package; 450 ns. max. cycle time; two chip selects.
- **R2332-3 32K STATIC ROM**
  Same as R2332, but has 300 ns. max. cycle time.



Input/Output Devices

General-Purpose I/O Devices

These versatile peripheral controllers allow effective trade-offs between software and hardware, enabling implementation of complex R6500 microcomputer systems at minimum overall cost. Both are available in 1 MHz and 2 MHz versions. All R6500 I/O devices—including the memory-I/O combos—have TTL and CMOS compatible peripheral lines with transistor drive capability and high-impedance, tri-state data outputs.

- **R6520 Peripheral Interface Adapter (PIA)**
  40-pin package, two 8-bit bi-directional I/O ports, four peripheral control/interrupt input lines, fully automatic data transfers between processor and peripheral devices.

The PIA provides individual I/O line control for keyboard strobes and returns, driving displays and discrete indicators as well as 8-bit parallel communications in *handshake* or clocked control modes.

- **R6522 Versatile Interface Adapter (VIA)**
  40-pin package, has R6520 PIA features plus two 16-bit programmable interval timers/counters, data latching on I/O ports, 8-bit buffered shift register for serial I/O interfacing.
  The enhanced features of the VIA provide a serial interface for inter-system communications, ASCII serial data generation, pulse width modulation, and waveform synthesis. The two timers work in conjunction with the serial channel or may provide interval timing for real time applications.

Memory-I/O-Timer Combination Devices

By combining an R650X Series CPU with one-chip memory, I/O and timer combination devices, the designer nets a powerful, cost-effective two chip microcomputer system which can also be the base configuration for modular, expandable applications.

- **R6530 ROM-RAM-I/O-Timer (RRIOT)**
  40-pin package; 1 MHz operation; 1024 x 8 ROM; 64 x 8 static RAM; two 8-bit bi-directional data I/O ports; two progammable data direction registers; programmable 8-bit interval timer with prescale and interrupt control.
- **R6531 ROM-RAM-I/O-Counter (RRIOC)**
  40-pin package; 1 MHz or 2 MHz operation; 2048 x 8 ROM; 128 x 8 static RAM; 8-bit serial data channel; two bi-directional I/O ports, with a total of 15 data lines, including four external interrupts and handshake control.

  The RRIOC also provides a fully-buffered 16-bit counter/timer with four program selectable modes — interval timer, pulse generator, event counter and pulse width measurement.

  A separate 52-pin version of RRIOC offers expanded I/O in additional 8-bit output port and 4-bit input port.
- **R6532 RAM-I/O-Timer (RIOT)**
  40-pin package; 1 MHz operation; 128 x 8 static RAM; two 8-bit bi-directional data ports; two programmable data direction registers; programmable 8-bit interval timer with prescale and interrupt control; programmable edge detect interrupt, for fast service of critical events.
- **R6534 ROM-I/O-Counter (RIOC)**
  40-pin package; 1 MHz operation; 4096 x 8 ROM; 8-bit serial data channel; two bi-directional data I/O ports, with a total of 14 data lines, including four external interrupts and handshake control.

  The RIOC also provides a programmable 16-bit counter/latch with interval timer, pulse generator and event counter modes.

  A separate 52-pin version of RIOC offers an additional 8-bit output port, 3-bit input port and one additional I/O line.

Intelligent Peripheral Controller Devices

The devices listed below get your interface design off to a solid start.

- **R6541 Programmable Keyboard/Display Controller (PKDC)**
  40-pin package, 8-character FIFO/Sensor RAM for keyboard entries, two CPU-addressable 16-byte display RAMs.

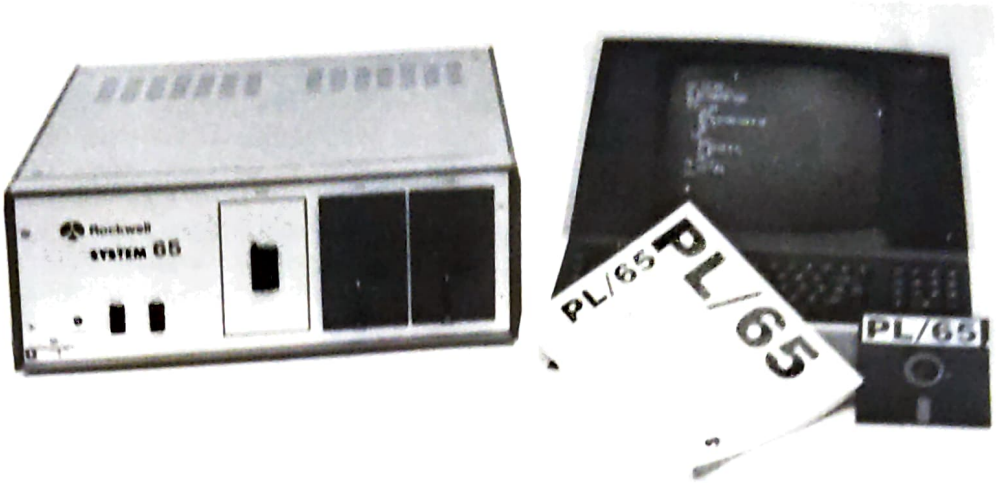
  The PKDC is a general-purpose keyboard and segmented display interface device. The keyboard portion can scan up to 128 matrix-type key switches, and can also interface with an array of 64 sensors or a strobed interface keyboard. The display portion provides a buffered scanned display interface with LED, fluorescent, Borroughs SELF-SCAN® , and other display technologies.
- **R6545 CRT Controller (CRTC)**
  40-pin package, refresh RAM, fully-programmable scanning and cursor, light pen register.

  The CRTC is designed to interface an 8-bit microprocessor to CRT raster scan video displays. It provides refresh memory addresses and character generator row addresses, which allow up to 16K characters with 32 scan lines per character to be addressed. Refresh memory may be addressed in either straight binary or by row/column.

Communications Interface Device

- **R6551 Asynchronous Communication Interface Adapter (ACIA)**
  28-pin package provides the interface between R6500-based systems and serial communication data sets and modems. With its on-chip baud rate generator, the ACIA is capable of transmitting at 15 different program-selectable rates between 50 baud and 19,200 baud, and receiving at either the transmit rate or at 16X an external clock rate.

  The ACIA has programmable word lengths of 5, 6, 7 or 8 bits; even, odd or no parity; 1, 1-1/2 or 2 stop bits.



Rockwell's SYSTEM 65

SYSTEM 65 is a new easy to use, powerful, complete development system for the R6500 family of microcomputers. The basic configuration includes two built-in, mini-floppy disk drives, 16K bytes of user memory and 16K bytes of resident operating system.

Monitor commands are self-prompting whenever memory, peripheral, or disk file assignment is required. Text editor provides line, string, and character editing functions. A resident two-pass assembler and dynamic debug package complete the operating system. Both source and object code may be maintained in memory for fast editing, assembling, and checkout. Since the total monitor, editor, debug and assembler are resident in ROM, 100% of the disk storage and drive utilization is available to the user.

The mini-floppy diskettes may be used as storage for source and object code and documentation. Each diskette has the capacity for 78K bytes of information in a maximum of 60 files.

SYSTEM 65 supports a variety of terminals with serial data from 100 baud to 9600 baud. Connectors are provided for both RS-232 C and current loop interfacing. Reader ON/OFF signals and RTS/CTS control signals are standard. Included is a parallel port providing automatic control to high speed printers, such as Diablo, Centronics and Tally.

And Rockwell offers these options to SYSTEM 65:

- PL/65 High-Level Language
- USER 65 in-circuit emulation option
- PROM Programmer Module, for programming a 2704/2708/2716/2758 PROM device from the front panel socket
- R6500/1 Personality option, for developing with the R6500/1 single-chip microcomputer
- 16K x 8 Static RAM Modules
- PROM/ROM Module, accepts 2316/2332 ROM or 2708/2716/2758 PROM devices
- Wire-wrap Design Prototyping Module
- Extender Card for circuit probing

PL/65 High-Level Language

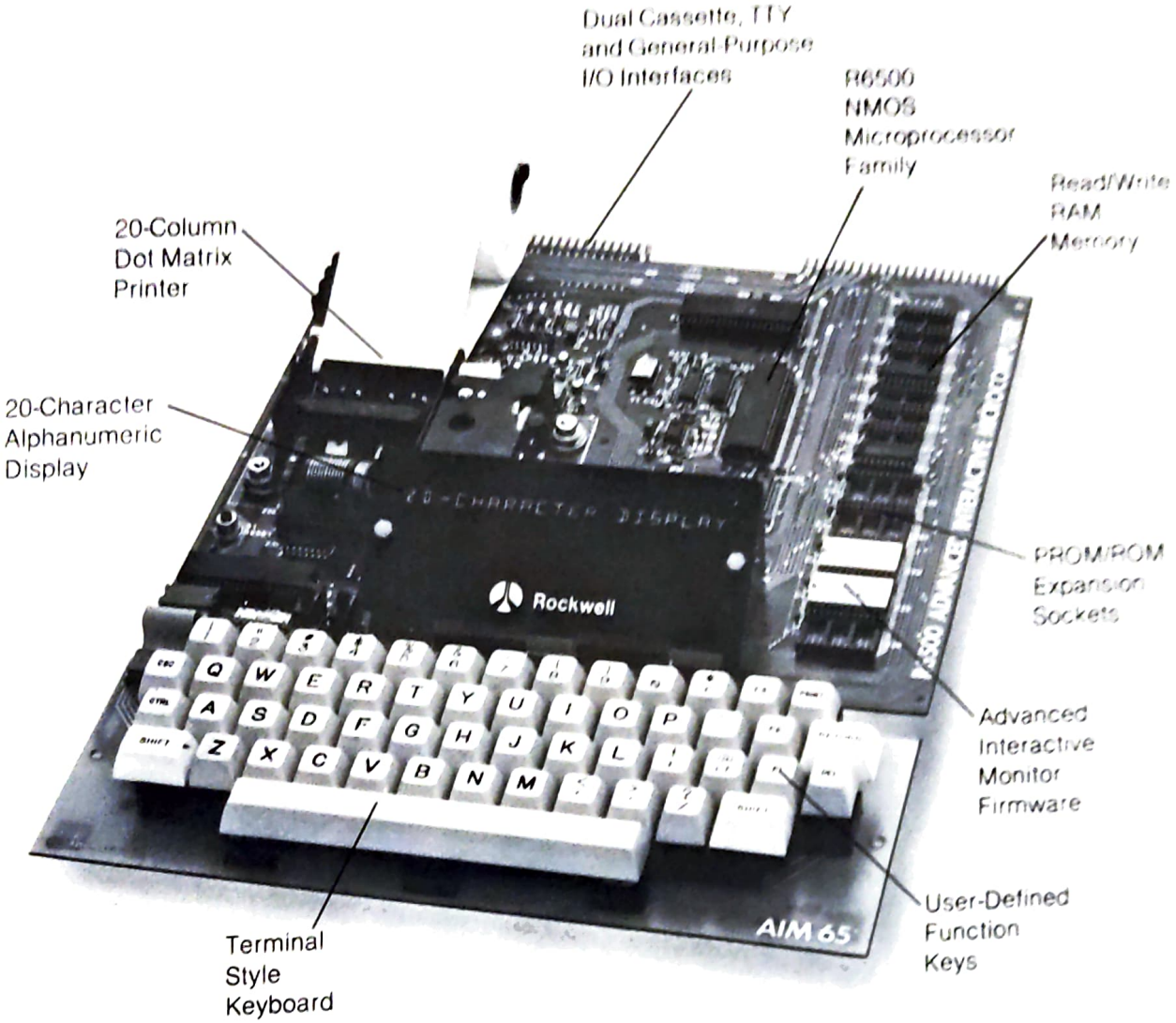
A high-level language resembling PL/1 and ALGOL is now available to designers developing programs for the R6500 microprocessor family using the SYSTEM 65 development system.

Designated PL/65, the language is considerably easier to use than assembly language or object code, thus increasing programmer productivity while reducing software development time and costs. The PL/65 compiler outputs source code to the SYSTEM 65's resident assembler. This permits enhancing or debugging at the assembler level before object code is generated. In addition, PL/65 statements may be mixed with assembly language instructions for timing or code optimization.

The PL/65 compiler is available to SYSTEM 65 users as a preprogrammed mini-floppy diskette. No additional memory is required other than the standard 16K bytes of RAM.

The PL/65 language supports modular program design. Its general control structures for conditional and iterative looping allow the language to be used effectively for structured programs. Other language features include: assignment, integer arithmetic, conditional execution, collective execution, linear array manipulation, data area declaration and array initialization. Block structures, subscripts and parenthetical expressions are also supported.

For learning, designing, work or just plain fun. . . .



Rockwell's R6500 Advanced Interactive Microcomputer (AIM 65) can get you into the exciting world of microcomputers a lot easier and at a lot lower cost than you may have thought possible.

As a learning aid, AIM 65 gives you an assembled, tested and warranted R6502-based microcomputer system with a full-sized keyboard, an alphanumeric 20-character display and, uniquely, an alphanumeric 20-column thermal printer.

An on-board Advanced Interactive Monitor program provides extensive control and program development functions. You'll be writing your programs in assembly language — there's no need to memorize "opcodes". And for more specialized applications, we offer a two-pass, symbolic assembler and a BASIC interpreter as plug-in ROM options.

You'll master fundamentals rapidly. Then you'll appreciate the fact that unlike the computer "toys" on the market, AIM 65 offers flexibility and expandability you would expect to find only in a sophisticated microcomputer development system.

Literature

How to make it all work for you

Rockwell has put together a complete set of documentation and reference manuals to help you implement the R6500 microprocessor family.

- **R6500 Hardware Manual**
  A detailed description of each chip in the family, how they interface, how the peripherals are controlled, as well as the design techniques facilitating system operation, testing and maintenance. Special emphasis is on "bringing up" a system with testing techniques, scope synchronizing and general trouble-shooting procedures — $5.
- **R6500 Programming Manual**
  Defines the architecture of the R6500 Series, the function of each instruction and valuable programming information. Special emphasis is on the sophisticated addressing modes of the family — $5.
- **Cross-Assembler Manual**
  Cross-Assembler directives are described as used in time-share and batch operations, with special aids on understanding and resolving error messages — $5.
- **SYSTEM 65 User's Manual**
  Instructs the user in operating the SYSTEM 65 Microcomputer Development System and its application in developing a working microprocessor system — $5.
- **PL/65 User's Manual**
  A complete guide to PL/65, the high-level language for the R6500 family — $10.
- **AIM 65 User's Guide**
  Full technical details tell you everything you need to operate the AIM 65 — $5.
- **AIM 65 BASIC Language Reference Manual**
  A how-to guide for using AIM 65 with the BASIC language ROM option installed—$5.
- **TIM Manual**
  Defines how to apply the Teletype I/O Monitor — $2.
- **R6500 Data Sheets**
  Provides quick understanding of the capabilities and characteristics of each available R6500 device and support equipment. To order data sheets simply specify the part number or the name of the support equipment.

Where to get more on the R6500

Rockwell's normal procedure is to provide you with free data sheets so that you can select the R6500 devices and support equipment of most interest to you. A nominal charge is made for reference manuals.

For data, devices or support equipment contact the nearest Rockwell office or distributor listed on the back page of this brochure. For in-depth assistance, obtain the name of your nearest Rockwell sales representative from any Rockwell office.